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IEC 1000-4-2 ESD Immunity and Transient Current Capability for the SP72X Series Protection Arrays

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The SP720, SP721, SP723, and SP724 are protection ICs with an array of SCR/Diode bipolar structures for ESD and over-voltage protection of sensitive input circuits. They have 2 protection SCR/Diode device structures per input. The SP720 is supplied in 16 lead DIP and SOIC packages and has a total of 14 available inputs that can be used to protect up to 14 external signal or bus lines. The SP721 and SP723 are 8 pin devices with the same protection structures and have the same package options. The SP723 has dual cell structures for each input to achieve substantially improved ESD and Transient Current capability. The SP724 is a four section array in a 6-lead SOT-23. Its cell structure has been redesigned for improved ESD immunity.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (positive supply terminal) or a $-V_{BE}$ diode threshold below V- (negative or ground). A clamp to V+ is activated at each protection input if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an input.

Various standards for testing the ESD capability of semiconductor products have been developed in recent years. Each standard was generated with regard to a specific need related to the electromagnetic compatibility of the system environment. They include the Human Body Model (HBM), Machine Model (MM) and the Charged Device Model (CDM). Each such standard relates to the nature of electrostatic discharge generated within a system application and the potential for damage to the IC. For these better known standards, the actual results for ESD tests on the SP720 and SP721 are as follows:

1. Human Body Model using a modified version of the MIL-STD-883, Method 3015.7; with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed all test levels from ±9kV to ±16kV (1kV steps).
2. Human Body Model using the MIL-STD-883, Method 3015.7 (with V- only grounded) and ESD discharge applied to each individual IN pin - Passed all test levels to ±6kV, failed ±7kV (1kV steps).
3. Machine Model using EIAJ IC121 ($R_D = 0\Omega$); discharge applied to IN pins with all others grounded - Passed all test levels to ±1kV, failed ±1.2kV; (200V steps).
4. Human Body Model using the IEC 1000-4-2 standard with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed test Level 2.

The SP723 capability surpasses those of the SP720 and SP721 and meets the Level 4 requirements of the IEC 1000-4-2 HBM standard.

IEC 1000-4-2 ESD Standard

One of the more recent standards to be developed is the IEC (International Electrotechnical Commission) 1000-4-2. The IEC document relates to the HBM but encompasses a range of normal environmental conditions. Testing for ESD immunity is more broadly defined to include a device, equipment or system. Both direct contact and air discharge methods of testing are used with four discrete steps in the severity level ranging up to 8kV and 15kV respectively. In its simplest form, the Figure 1 test circuit provides for a means of charging the 150pF capacitor, R_C through the charge switch and discharging ESD pulses through the 330Ω resistor, R_D and discharge switch to the Equipment or Device Under Test (EUT, DUT) under test.

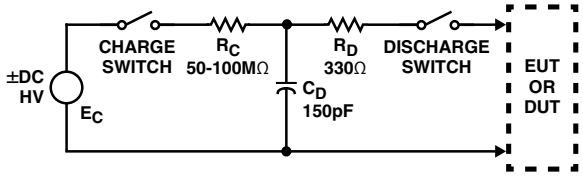

FIGURE 1. SIMPLIFIED IEC 1000-4-2 ESD TEST ENERGY SOURCE

The test equipment for the IEC 1000-4-2 standard is constructed to provide the equivalent of an actual human body ESD discharge and has the waveform shown in Figure 2.

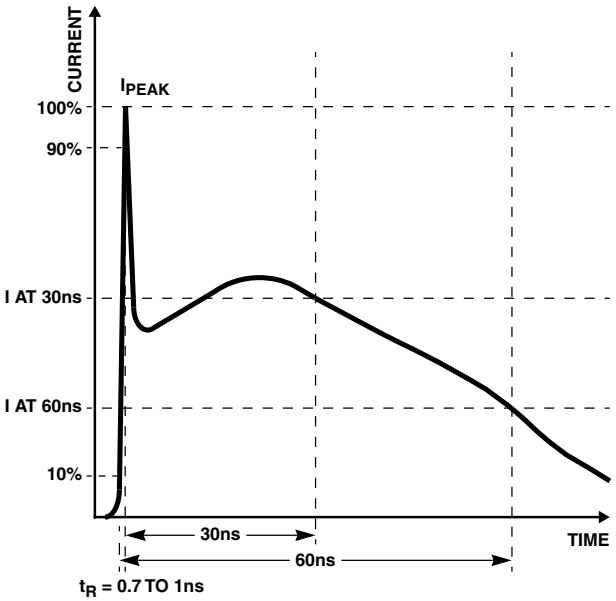

FIGURE 2. TYPICAL WAVEFORM OF THE OUTPUT CURRENT OF THE HBM ESD GENERATOR AS SPECIFIED IN THE IEC 1000-4-2 STANDARD

The IEC 1000-4-2 severity level of testing is defined by stepping the DC High Voltage rather than changing the R_C discharge components. The severity levels are separately defined for plus and minus polarity of direct contact discharge (preferred) and air discharge as shown in Table 1. Other voltage levels may be specified for the IEC 1000-4-2 test equipment and conditions.

TABLE 1. IEC 1000-4-2 SEVERITY LEVELS

LEVEL	TEST VOLTAGE, kV CONTACT DISCHARGE	TEST VOLTAGE, kV AIR DISCHARGE
1	2	2
2	4	4
3	6	8
4	8	15

As a subsystem component, the SP720, SP721 and SP723 may be used at the PC board or module interface for protection. In a typical application, the ESD Protection Arrays would be used to protect more sensitive circuits at the line interface or input terminals to a board or module.

Normally, the circuit configuration of Figure 3 is the recommended way to protect ESD sensitive inputs which relates to the IEC 1000-4-2 definitions for equipment, systems, subsystems and peripherals. To determine the capability of ESD Protection Arrays to protect an active circuit, the ESD Protection Arrays were tested as single devices. Following the conditions of the IEC 1000-4-2 specification, both direct contact and air discharge ESD tests were performed.

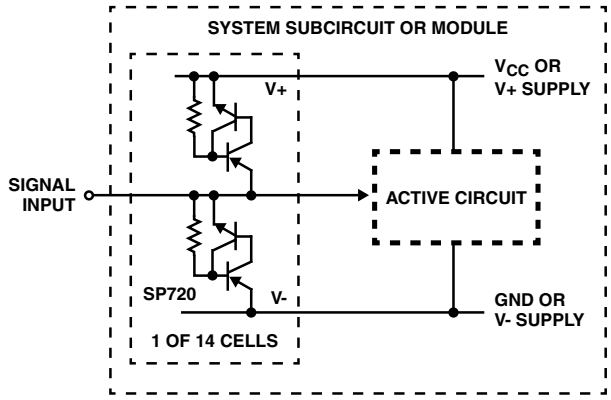

FIGURE 3. ONE PROTECTION CELL OF THE SP720 SHOWN AS PROTECTION INTERFACE ON A CIRCUIT

IEC 1000-4-2 ESD Test Evaluation

ESD Direct Contact and Air Discharge Capability

For V- = Ground, V+ = V_{CC} (varied) and $T_A = 25^oC$, single pulse ESD testing was done at each pin of the SP720 and SP721. The results are shown in Tables 2A and 2B. In general, the SP720 and SP721 have the capability to withstand Level 2 direct contact ESD discharge for the test conditions defined in the IEC 1000-4-2 standard.

In Table 2C, all pins on six SP720 and four SP721 devices were tested for ESD Air Discharge Capability and passed without failures up to 16.5kV. This is better than the IEC 1000-4-2 standard to Level 4 severity requirements. The SP723 was tested using the same conditions given for the SP720 and SP721.

TABLE 2A. SP720 TESTS TO IEC 1000-4-2 STRESS LEVELS USING DIRECT CONTACT

STRESS LEVELS	(+) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 0V, 5 Devices Tested		
1, 2, 3	All Pass	All Pass
4	All Pass	2 Fail
V_{CC} = 5.5V, 20 Devices Tested		
1, 2	All Pass	All Pass
3	All Pass	8 Fail
4	All Pass	Remaining 12 Fail
V_{CC} = 15V, 6 Devices Tested		
1, 2	All Pass	All Pass
3	All Pass	3 Fail
4	All Pass	Remaining 3 Fail

TABLE 2B. SP721 TESTS TO IEC 1000-4-2 STRESS LEVELS USING DIRECT CONTACT

STRESS LEVELS	(+) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 5.5V, 20 Devices Tested		
1, 2	All Pass	All Pass
3	All Pass	8 Fail
4	All Pass	Remaining 12 Fail

TABLE 2C. SP720 AND SP721 TESTS TO IEC 1000-4-2 STRESS LEVELS USING AIR DISCHARGE

STRESS LEVELS	(+) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 15V, 6 SP720, 4 SP721 Devices Tested		
1	All Pass	All Pass
2	All Pass	All Pass
3	All Pass	All Pass
4	All Pass	All Pass

The SP723 was tested using the same conditions given for the SP720 and SP721.

Table 2D shows the results for direct contact discharge and Table 2E show the SP723 capability for air discharge. Where each SP723 input has a dual input structure equal to the SP720 and SP721 which pass Level 4 air discharge conditions, the capability of the SP723 will exceed that by a wide margin but testing was not done due to test equipment limitations.

TABLE 2D. SP723 TESTS TO IEC 1000-4-2 STRESS LEVELS USING DIRECT DISCHARGE

STRESS LEVELS	(+) DIRECT DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) DIRECT DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 15V, 8 Devices Tested		
1, 2, 3, 4	All Pass	All Pass

TABLE 2E. SP723 IEC 1000-4-2 STRESS LEVEL CAPABILITY USING AIR DISCHARGE

STRESS LEVELS	(+) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN
Results based on SP720, SP721 Data		
1, 2, 3, 4	All Pass	All Pass

Measured Peak Current in Direct Discharge ESD Testing

Verification for peak current calibration during testing for the ESD direct contact discharge was done for ESD Tests in Table 2. The measured peak currents occurs in 1ns and the 50% discharge occurs in 30ns as shown in Figure 2. The verified results as shown below in Table 3. These test levels conform to the IEC 1000-4-2 standard requirement for peak current to be within ±10%.

TABLE 3. SP720 TESTS TO IEC 1000-4-2 VOLTAGE LEVELS

LEVEL	VOLTAGE	PEAK CURRENT 0.7ns TO 1ns RISE TIME, MEASURED	PEAK CURRENT 0.7ns TO 1ns RISE TIME, STANDARD
Level 1	+2kV -2kV	+7.5A -8A	±7.5A
Level 2	+4kV -4kV	+15A -16A	±15A
Level 3	+6kV -6kV	+22A -22A	±22.5A
Level 4	+8kV -8kV	-	±30A at 8kV
Level 4 plus 1kV	+9kV -9kV	+34A -34A	

The 9kV level was measured (instead of 8kV) to verify the extended range level of performance, which is the limit of the test equipment. A linear increase beyond the specified standard of 30A at 8kV would be equivalent to 33.75A at 9kV.

Multiple Pin Input ESD Test Evaluation

While the SP723 would be a preferred choice to extend the range of ESD protection, by using 2 or more IN input pins of the SP720 or SP721 also increases the range of ESD immunity. For example, by connecting adjacent SP720 pins in parallel using the dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15, the IEC 1000-4-2 voltage capability is increased to better than ±9kV. (The ±9kV level is an equipment limited maximum voltage.)

Peak Current Capability

While the primary purpose of the SP720, SP721 and SP723 are for ESD protection, there is an implied need for surge current immunity in some circuit applications. As noted by the high peak currents recorded during ESD testing (Table 3), it can be expected that peak transient current capability rises sharply as the width of the current pulse narrows.

Destructive testing was done to fully evaluate device ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4. The test circuit of Figure 4 is shown with a positive pulse input as it would apply to the SP720. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.)

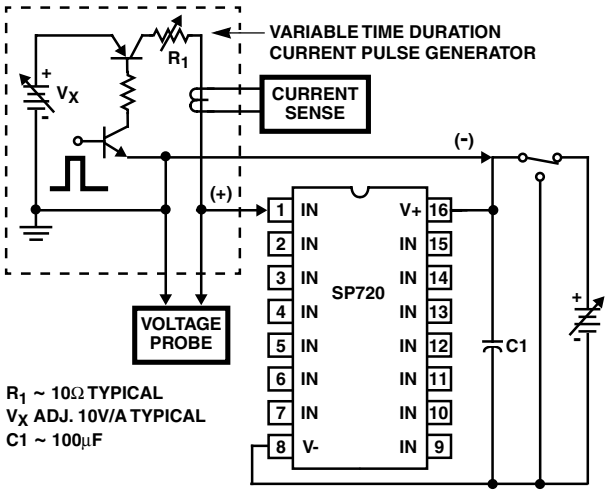

FIGURE 4. TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

Figure 5 shows a connected curve for each point of overstress as defined by increased leakage in the SP720 to well over the published limits of the data sheet. Using the similar connection test circuit configuration, the SP723 capability is shown on the same curve. The SP723 curve for a 15V supply shows a capability of 10A peak current for the 10µs pulse and 4A peak current for the 1ms pulse. The complete curve for a single pulse time up to 1 second is shown.

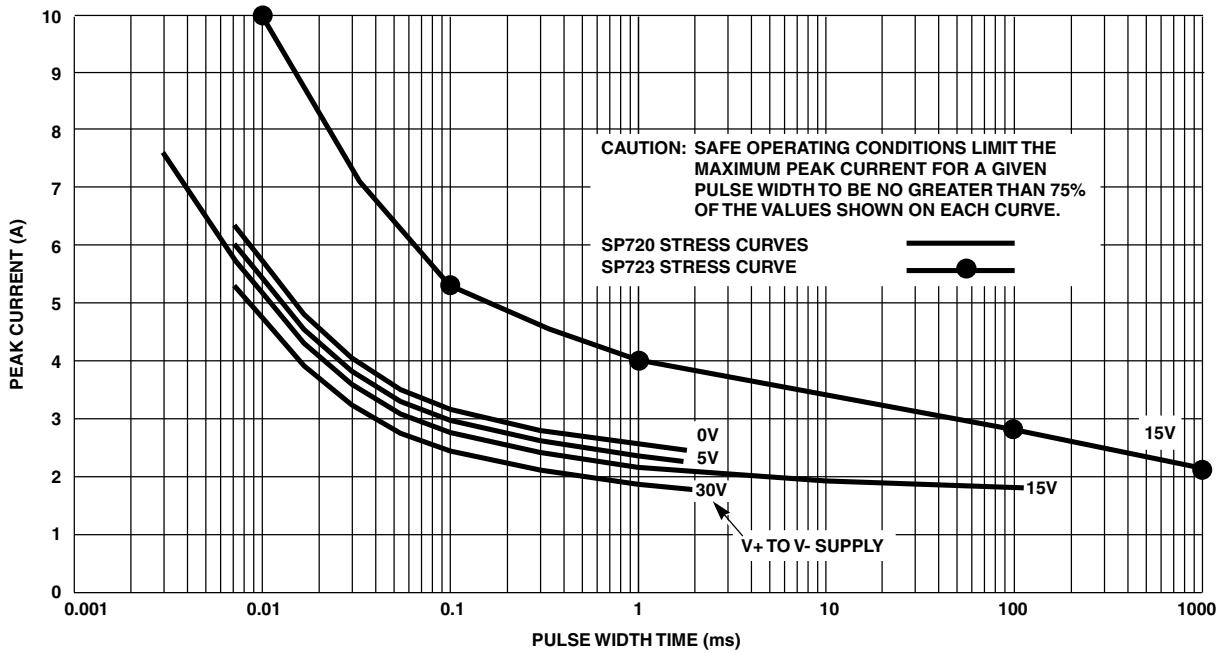

FIGURE 5. SP720 AND SP723 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVERSTRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS (T_A = 25°C)

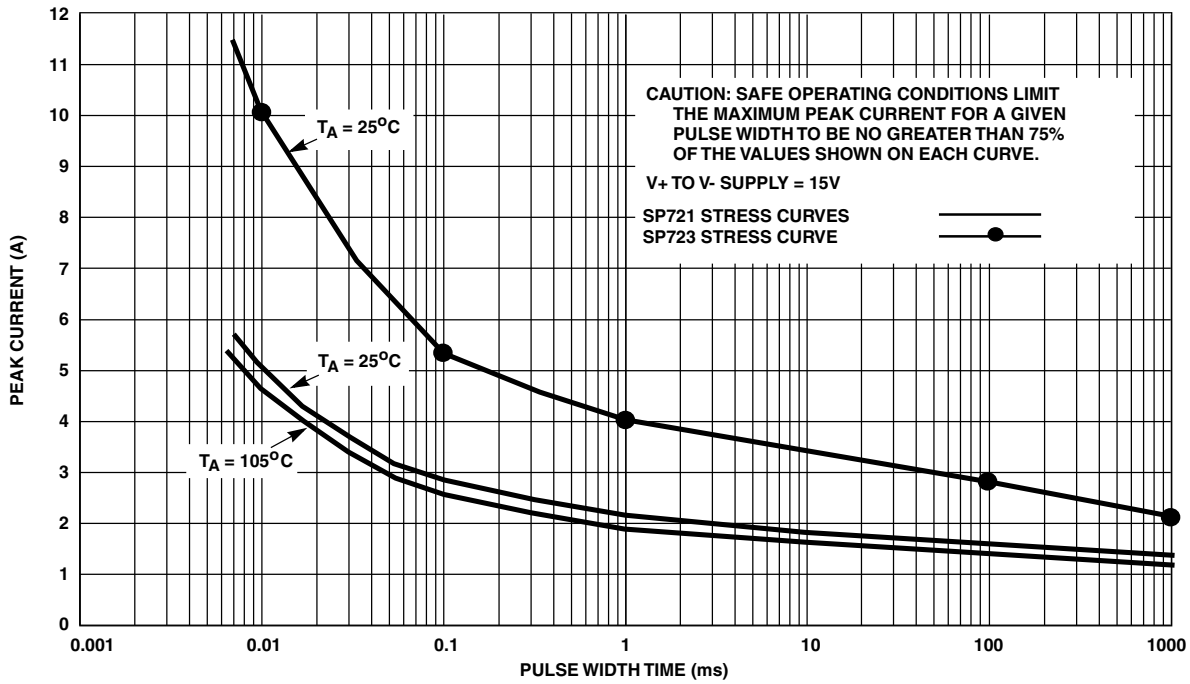

FIGURE 6. SP721 AND SP723 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVERSTRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS

Figure 6 shows the single pulse peak current capability of the SP721 for 105°C ambient temperature conditions. The SP721 is an 8 pin package version of the SP720 but is otherwise has the same short pulse width peak current capability. The SP721 curve for 25°C is shown for comparison. The reduction in maximum peak current attributed to an increase of ambient temperature from 25°C to 105°C is typically 10%. The overall effect of increased chip temperature, whether by ambient temperature increase or current induced dissipation, is to reduce the peak current ratings. The maximum rated operating ambient temperature for both the SP720 and SP721 is 105°C.

Multiple Pin Input Peak Current Test Evaluation

Uniformity of design and processing in the SP720 provides the capability to use multiple pins for added input protection. The very short pulse test capability for the dual pins is approximately twice the peak current for a single pin. However, for the 100ms to 1000ms pulses, the dual pin peak current stress capability decreases, approaching that of the single pin level. The longer pulse condition is limited by the heat capacity of the chip and eventually forces a more rapid increase in the chip temperature.

Other Transient Conditions

Conducted Susceptibility to Transients

Conducted Susceptibility to Transients is a test defined by the automotive SAE J1113 standard. The waveform used to test devices simulates the transient caused by a parallel or series inductive load when the supply current is switched off. Figure 7 illustrates the pulse waveforms generated by a Schaffner 5000 Transient Pulse Test Generator used to test the SP720. For the purposes of this test, Test Pulse 1 and 2 were applied while the V+ and V- voltage to the SP720 was at ground. Destructive level testing at room temperature was conducted with a single 200µs pulse while applying the transient signal to each IN input pin. It should be noted that the width for the 200µs pulse is defined for the 10% turn-on levels. The sourced voltage from the generator, V_S, was varied while the peak current was monitored.

Test Results for Single Pin Testing

Up to 10 consecutive pulses were applied at a 5 second rate to verify the transient capability of each input. It was determined that levels of +5.5A and -8A were sufficient to damage the inputs. Peak current levels of +5A (+6.5V) and

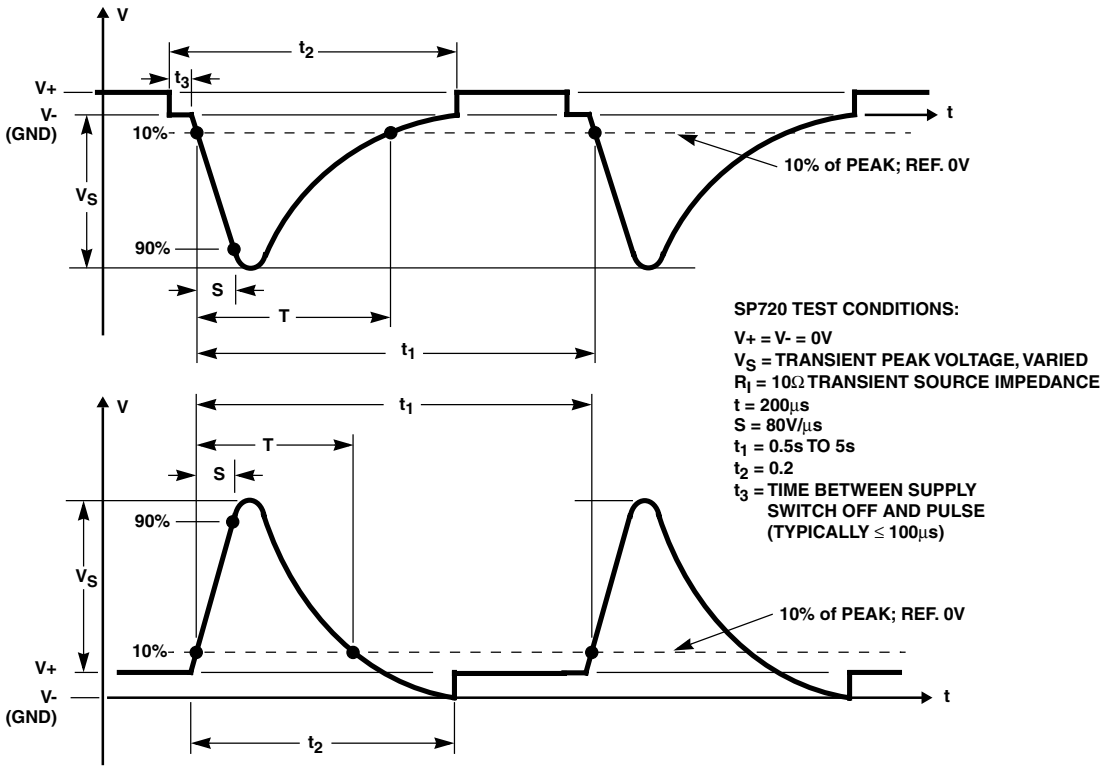

FIGURE 7. TRANSIENT INDUCTIVE DISCHARGE VOLTAGE vs TIME WAVEFORMS APPLIED TO THE SP720 INPUT 'IN' PINS. THE TOP WAVEFORM IS APPLIED FOR THE A DUT IN PARALLEL WITH AN INDUCTIVE LOAD AND THE BOTTOM WAVEFORM IS APPLIED FOR SERIES CONNECTED POWER TURN-OFF (REF. SAE J1113 STANDARD)

-7A (-6V) were found to be a marginal safe level for single pulses applied to the IN inputs.

Test Results for Double Pin Testing

It was determined that paralleling input pins will permit twice the single pin current capability. Sustained testing at a 2Hz rate was done after paralleling pins 1+2, 3+5 and 6+7. The results for a +10A, 200µs positive transient current pulse were:

PINS IN PARALLEL	1+2	3+5	6+7	
Device 2 Failed at	-	3500	5600	Pulses
Device 3 Failed at	1150	230	340	Pulses

Sustained safe peak current levels should be no more than 70% of the point of overstress. At higher ambient temperature up to the maximum rated conditions of 105°C, the allowed maximum peak current should be further reduced by at least 10%.

SP720 and SP723 Surge Immunity Test Capability per the 8/20µs Short Circuit Conditions of IEC 1000-4-5

While the IEC 1000-4-5 is a standard that generally implies higher levels of power than recommended for the SP720 and SP723, testing was done to determine the comparable level of capability. The test circuit conditions for an 8/20µs short circuit current pulse are shown in Figures 8A and 8B. It should be noted that the 8/20µs pulse is defined as 20µs wide from a delayed turn-on to a 50% turn-off.

SP720 Test Results: The short circuit current marginal point of overstress at room temperature was determined to be:

For +IN Positive Surge Polarity (upper unit):
- V_{CC} = 6V Typically greater than 5A
- V_{CC} = 15V Typically greater than 4.8A
- V_{CC} = 35V Typically greater than 4.2A

For -IN Negative Surge Polarity (lower unit):
- V_{CC} = 15V Typically greater than 5.8A
- V_{CC} = 35V Typically greater than 5.8A

As previously noted, paralleling pins on the SP720 will increase the current capability to approximately twice that of a single IN pin.

SP723 Test Results: The short circuit current marginal point of overstress at room temperature was determined to be:

For +IN Positive Surge Polarity (upper unit):
- V_{CC} = 6V Typically greater than 9.8A
- V_{CC} = 15V Typically greater than 9.5A
- V_{CC} = 35V Typically greater than 9A

For -IN Negative Surge Polarity (lower unit):
- V_{CC} = 6V Typically greater than 11.7A
- V_{CC} = 15V Typically greater than 11.1A
- V_{CC} = 35V Typically greater than 10.6A

As previously noted, sustained safe peak current levels should be no more than 70% of the point of overstress. At higher ambient temperature up to the maximum rated conditions of 105°C, the allowed maximum peak current should be further reduced by at least 10%.

R_C CHARGING RESISTOR
C_C ENERGY STORAGE CAPACITOR
R_{S1}, R_{S2} PULSE SHAPING RESISTORS
L_R RISETIME SHAPING INDUCTOR

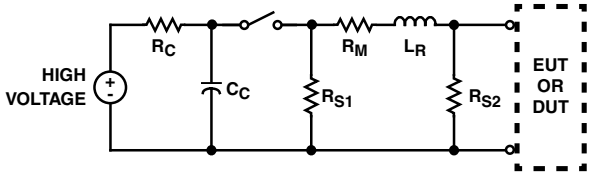

FIGURE 8A. CIRCUIT DIAGRAM OF GENERATOR FOR 8/20µs PULSE WAVEFORM

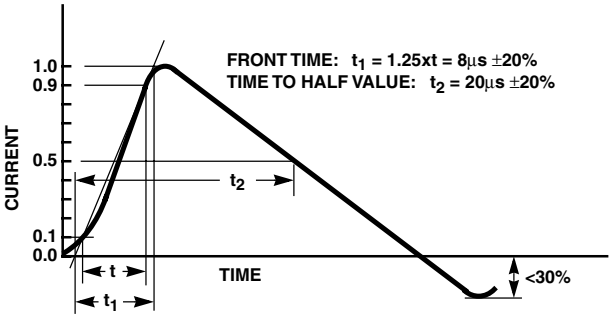

FIGURE 8B. WAVE SHAPE FOR 8/20µs SHORT CIRCUIT CURRENT PULSE PER IEC 60-1